WHAT IS CLAIMED IS:

1. An active matrix substrate comprising:

a base substrate;

a plurality of gate lines formed on the base substrate;

a plurality of data lines, each said data line crossing all of the gate lines with a first insulating film interposed therebetween;

a plurality of thin-film transistors formed over the base substrate, each said thin-film transistor being associated with one of the gate lines and operating responsive to a signal on the associated gate line; and

a plurality of pixel electrodes, each said pixel electrode being associated with one of the data lines and one of the thin-film transistors and being electrically connectable to the associated data line by way of the associated thin-film transistor,

wherein each said pixel electrode and the associated thin-film transistor are connected together by way of a conductive member, and

wherein each said pixel electrode crosses one of the gate lines, while the conductive member for the pixel electrode crosses another one of the gate lines that is adjacent to the former gate line.

2. The active matrix substrate of claim 1,further com-

prising a plurality of storage capacitance lines formed on the base substrate; each said data line crossing all of the date lines with a second insulating film interposed therebetween;

wherein each said pixel electrode crosses not only one of the gate lines but also one of the storage capacitance lines, while the conductive member for the pixel electrode crosses not only another one of the gate lines that is adjacent to the former gate line but also another one of the storage capacitance lines that is adjacent to the former storage capacitance line.

3. An active matrix substrate comprising:

a base substrate;

a plurality of gate lines formed on the base substrate;

a plurality of data lines, each said data line crossing all of the gate lines with a first insulating film interposed therebetween;

a plurality of thin-film transistors formed over the base substrate, each said thin-film transistor being associated with one of the gate lines and operating responsive to a signal on the associated gate line;

a plurality of lower-level pixel electrodes, each said lower-level pixel electrode being associated with one of the data lines and one of the thin-film transistors and being

electrically connectable to the associated data line by way of the associated thin-film transistor; and

a plurality of upper-level pixel electrodes located over the lower-level pixel electrodes with a second insulating film interposed therebetween, each said upper-level pixel electrode being associated with, and electrically connected to, one of the lower-level pixel electrodes by way of an associated contact hole,

wherein each said upper-level pixel electrode and the associated lower-level pixel electrode together makes up a pixel electrode, which is connected to the thin-film transistor, associated with the lower-level pixel electrode, by way of a conductive member, and

wherein the data lines, the conductive members and the lower-level pixel electrodes have all been formed by patterning the same conductive film, and

wherein each said lower-level pixel electrode crosses one of the gate lines, while the conductive member for the lower-level pixel electrode crosses another one of the gate lines that is adjacent to the former gate line.

4. The active matrix substrate of claim 3, further comprising a plurality of storage capacitance lines formed on the base substrate; each said data line crossing all of the date lines with a second insulating film interposed therebe-

tween;

wherein each said lower-level pixel electrode crosses not only one of the gate lines but also one of the storage capacitance lines, while the conductive member for the lower-level pixel electrode crosses not only another one of the gate lines that is adjacent to the former gate line but also another one of the storage capacitance lines that is adjacent to the former storage capacitance line.

5. An active matrix substrate comprising:

a base substrate;

a plurality of gate lines formed on the base substrate;

a plurality of auxiliary capacitance lines formed on the base substrate;

a plurality of data lines, each said data line crossing all of the gate and auxiliary capacitance lines with a first insulating film interposed therebetween;

a plurality of thin-film transistors formed over the base substrate, each said thin-film transistor being associated with one of the gate lines and operating responsive to a signal on the associated gate line;

a plurality of lower-level pixel electrodes, each said lower-level pixel electrode being associated with one of the data lines and one of the thin-film transistors and being electrically connectable to the associated data line by way of

the associated thin-film transistor; and

a plurality of upper-level pixel electrodes located over the lower-level pixel electrodes with a second insulating film interposed therebetween, each said upper-level pixel electrode being associated with, and electrically connectable to, one of the lower-level pixel electrodes by way of an associated contact hole,

wherein each said upper-level pixel electrode and the associated lower-level pixel electrode together makes up a pixel electrode, which is connected to the thin-film transistor, associated with the lower-level pixel electrode, by way of a conductive member, and

wherein the data lines, the conductive members and the lower-level pixel electrodes have all been formed by patterning the same conductive film, and

wherein when one of the gate lines crosses associated ones of the lower-level pixel electrodes, one of the auxiliary capacitance lines, which is adjacent to the gate line, crosses associated ones of the conductive members, and

wherein when one of the gate lines crosses associated ones of the conductive members, one of the auxiliary capacitance lines, which is adjacent to the gate line, crosses associated ones of the lower-level pixel electrodes.

6. The active matrix substrate of claim 5, further comprising source electrodes, each said source electrode branching from one of the data lines and crossing one of the gate lines,

wherein an intersection of each said conductive member with associated one of the gate lines is located between an intersection of one of the data lines that is closest to the conductive member and the gate line and an intersection of one of the source electrodes that is closest to the conductive member and the gate line.

7. The active matrix substrate of claim 6, wherein a distance between each said conductive member and the data line closest to the conductive member is substantially equal to a distance between the conductive member and the source electrode closest to the conductive member.

8. The active matrix substrate of claim 7, wherein each said thin-film transistor has its channel located substantially at the midpoint between two adjacent ones of the data lines.

9. The active matrix substrate of claim 8, wherein the channel of each said thin-film transistor is covered with one of the upper-level pixel electrodes.

10. The active matrix substrate of claim 1, 3, or 5, wherein a semiconductor layer for each said thin-film transistor has been self-aligned with the gate line associated with the thin-film transistor, and

wherein the data lines and associated ones of the conductive members cross the semiconductor layer.

11. The active matrix substrate of claim 10, wherein the channel regions in the semiconductor layer are covered with a channel protective layer that has been self-aligned with the associated gate line.

12. The active matrix substrate of claim 11, wherein side faces of the channel protective layer, which are parallel to a direction in which the data lines and the conductive members extend, are aligned with outer side faces of the data lines and the conductive members.

13. The active matrix substrate of claim 12, wherein the other side faces of the channel protective layer, which are parallel to a direction in which the gate lines extend, are spaced apart from each other by a distance smaller than the line width of the gate lines.

14. The active matrix substrate of claim 1, 3, or 5, wherein each said conductive member extends from the pixel electrode, connected to the conductive member, parallel to the data lines, and

wherein a distance between a far end of the conductive member and an opposite far end of the pixel electrode, connected to the conductive member, is longer than a pitch of the gate lines but less than twice as long as the gate line pitch.

15. The active matrix substrate of claim 1, 3, or 5, wherein each of the data lines, the conductive members and the pixel electrodes includes a conductive layer that has been formed by patterning the same conductive film.

16. The active matrix substrate of claim 1 or 2, wherein each of the data lines, the conductive members and the pixel electrodes includes a transparent conductive layer that has been formed by patterning the same transparent conductive film, and

wherein an opaque film covers the transparent conductive layer included in each said data line.

17. The active matrix substrate of claim 16, wherein the opaque film is made of a metal that has an electrical resis-

tivity lower than that of the transparent conductive layer.

18. The active matrix substrate of claim 1, 3, or 5, wherein in a display area, no parts of the gate and data lines protrude parallel to the surface of the base substrate.

19. The active matrix substrate of one of claims 1, 3, or 5, wherein the gate lines are made of a metal with opacity.

20. The active matrix substrate of claim 1, 3, or 5, wherein each said gate line has a slit-like opening that transmits light at least in respective areas where the thin-film transistors are formed.

21. The active matrix substrate of claim 1, 3, or 5, wherein each said gate line is divided into multiple line portions at least in respective areas where the thin-film transistors are formed.

22. The active matrix substrate of claim 21, wherein when a negative photosensitive resin layer, which has been formed to cover the gate lines, is partially exposed to light that has been incident thereon through the backside of the base substrate, each said line portion has such a line width

as exposing substantially all of the negative photosensitive resin layer, which is located over the line portion, to the light by utilizing diffraction of the light.

23. The active matrix substrate of claim 1, 3, or 5, wherein the data lines are laid out over the base substrate so as to allow the base substrate to expand or shrink less horizontally to the data lines than vertically to the data lines.

24. The active matrix substrate of claim 1, 3, or 5, wherein the gate lines are extended beyond the display area, and

wherein the extension of each said gate line has a length greater than the gate line pitch.

25. The active matrix substrate of claim 1, 3, or 5, wherein color filters have been formed over the pixel electrodes.

26. The active matrix substrate of claim 1, 3, or 5, wherein the base substrate is made of plastic.

27. The active matrix substrate of claim 26, wherein the base substrate comprises, as an integral part thereof, an op-

tical member for changing the optical path or polarization of incident light.

28. An active matrix substrate comprising:

a plastic substrate;

a first gate line formed on the plastic substrate;

a second gate line formed on the plastic substrate and placed parallel to the first gate line;

a third gate line formed on the plastic substrate and placed parallel to the second gate line;

a data line crossing the first, second and third gate lines with an insulating film interposed therebetween;

a first pixel electrode crossing the first gate line;

a second pixel electrode crossing the second gate line;

a first thin-film transistor self-aligned with the second gate line; and

a second thin-film transistor self-aligned with the third gate line,

wherein the first pixel electrode is connected to the first thin-film transistor by way of a first conductive member that crosses the second gate line, and

wherein the second pixel electrode is connected to the second thin-film transistor by way of a second conductive member that crosses the third gate line.

29. A display device comprising:

an active matrix substrate as recited in claim 1, 3,or 5;

a counter substrate facing the active matrix substrate; and

a light modulating layer interposed between the active matrix and counter substrates.

30. A portable electronic unit comprising a display device as recited in claim 29.

31. A method of making an active matrix substrate, comprising the steps of:

a) forming a plurality of gate lines on a base substrate;

b) depositing an insulating film that covers the gate lines;

c) depositing a semiconductor layer over the insulating film;

d) forming a positive resist layer over the semiconductor layer;

e) exposing the positive resist layer to light that has been incident thereon through the backside of the base substrate and then developing the positive resist layer exposed, thereby defining a first resist mask over the gate lines so

that the first resist mask is aligned with the gate lines;

f) removing parts of the semiconductor layer, which are not covered with the first resist mask, thereby forming a striped semiconductor layer, including portions to be semiconductor regions for thin-film transistors, so that the striped semiconductor layer is self-aligned with the gate lines;

g) removing the first resist mask;

h) depositing a conductive film over the striped semiconductor layer; and

i) patterning the conductive film using a second resist mask, thereby forming not only a data line and a pixel electrode, which both cross a first one of the gate lines, but also a conductive member, which extends from the pixel electrode parallel to the data line and crosses a second one of the gate lines that is adjacent to the first gate line, and then patterning the striped semiconductor layer, thereby defining the semiconductor regions for the thin-film transistors below the data line and the conductive member.

32. The method of claim 31, wherein the step i) comprises:

defining a resist pattern, which includes: relatively thick portions that will define the data line and the conductive member; and a relatively thin portion that will define a

region between the data line and the conductive member, as the second resist mask;

etching away parts of the conductive film and the striped semiconductor layer that are not covered with the resist pattern;

removing the relatively thin portion from the resist pattern; and

etching away another part of the conductive film, which has been covered with the relatively thin portion of the resist pattern, thereby forming the data line and the conductive member.

33. A method of making an active matrix substrate, comprising the steps of:

a) forming a plurality of gate lines on a base substrate;

b) depositing an insulating film that covers the gate lines;

c) depositing a semiconductor layer over the insulating film;

d) forming a positive resist layer over the semiconductor layer;

e) exposing the positive resist layer to light that has been incident thereon through the backside of the base substrate and then developing the positive resist layer exposed,

thereby defining a first resist mask over the gate lines so that the first resist mask is aligned with the gate lines;

f) removing parts of the semiconductor layer, which are not covered with the first resist mask, thereby forming a striped semiconductor layer, including portions to be semiconductor regions for thin-film transistors, so that the striped semiconductor layer is self-aligned with the gate lines;

g) removing the first resist mask;

h) depositing a transparent conductive film over the striped semiconductor layer;

i) depositing an opaque film over the transparent conductive film;

j) patterning the opaque and transparent conductive films using a second resist mask, thereby forming not only a data line and a pixel electrode, which both cross a first one of the gate lines, but also a conductive member, which extends from the pixel electrode parallel to the data line and crosses a second one of the gate lines that is adjacent to the first gate line, and then patterning the striped semiconductor layer, thereby defining the semiconductor regions for the thin-film transistors below the data line and the conductive member;

k) coating the surface of the base substrate with a negative photosensitive resin material; and

l) exposing the negative photosensitive resin material to light that has been incident thereon through the backside of the base substrate, and then developing the negative photosensitive resin material exposed, thereby removing non-exposed parts of the negative photosensitive resin material and forming a black matrix.

34. The method of claim 33, wherein in the step l), parts of the negative photosensitive resin material, which cover the data line, the conductive member and the semiconductor regions for the thin-film transistors, are exposed to light that passes through areas where the gate lines and the opaque film do not exist, thereby covering an area where the pixel electrode does not exist with the black matrix.

35. The method of claim 33 or 34, wherein parts of the opaque film, which are not covered with the black matrix, are etched away, thereby defining a translucent region over the pixel electrode.

36. The method of claim 35, wherein the step j) comprises:

defining a resist pattern, which includes: relatively thick portions that will define the data line and the conductive member; and a relatively thin portion that will define a

region between the data line and the conductive member, as the second resist mask;

etching away parts of the opaque film, the transparent conductive film and the striped semiconductor layer that are not covered with the resist pattern;

removing the relatively thin portion from the resist pattern; and

etching away another part of the opaque film and the transparent conductive film, which has been covered with the relatively thin portion of the resist pattern, thereby forming the data line and the conductive member.

37. A method of making an active matrix substrate, comprising the steps of:

a) forming a plurality of gate lines on a base substrate;

b) depositing an insulating film that covers the gate lines;

c) depositing a semiconductor layer over the insulating film;

d) forming a channel protective layer over the semiconductor layer;

e) forming a first positive resist layer over the channel protective layer;

f) exposing the first positive resist layer to light

that has been incident thereon through the backside of the base substrate and then developing the first positive resist layer exposed, thereby defining a first resist mask over the gate lines so that the first resist mask is aligned with the gate lines;

g) removing parts of the channel protective layer, which are not covered with the first resist mask, thereby patterning and self-aligning the channel protective layer with the gate lines so that the patterned channel protective layer has a line width narrower than that of the gate lines;

h) depositing a contact layer over the patterned channel protective layer and the semiconductor layer;

i) forming a second positive resist layer over the contact layer;

j) exposing the second positive resist layer to light that has been incident thereon through the backside of the base substrate and then developing the second positive resist layer exposed, thereby defining a second resist mask over the gate lines so that the second resist mask is aligned with the gate lines;

k) removing parts of the contact and semiconductor layers, which are not covered with the second resist mask, thereby forming a striped contact layer and a striped semiconductor layer, including portions to be semiconductor regions for thin-film transistors, so that the striped contact and

semiconductor layers are both self-aligned with the gate lines;

l) removing the second resist mask;

m) depositing a conductive film over the striped contact layer; and

n) patterning the conductive film using a third resist mask, thereby forming not only a data line and a pixel electrode, which both cross a first one of the gate lines, but also a conductive member, which extends from the pixel electrode parallel to the data line and crosses a second one of the gate lines that is adjacent to the first gate line, and then patterning the striped contact layer, the pattered channel protective layer and the striped semiconductor layer, thereby defining the semiconductor regions for the thin-film transistors below the data line and the conductive member so that the upper surface of the semiconductor regions is partially covered with the patterned channel protective layer.

38. The method of claim 37, wherein the step n) comprises:

defining a resist pattern, which includes: relatively thick portions that will define the data line and the conductive member; and a relatively thin portion that will define a region between the data line and the conductive member, as the third resist mask;

etching away parts of the conductive film, the striped contact layer, the patterned channel protective layer and the striped semiconductor layer that are not covered with the resist pattern;

removing the relatively thin portion from the resist pattern; and

etching away another part of the conductive film and contact layer, which has been covered with the relatively thin portion of the resist pattern, thereby forming the data line and the conductive member that are separated from each other.

39. A method of making an active matrix substrate, comprising the steps of:

a) forming a plurality of gate lines on a base substrate;

b) depositing an insulating film that covers the gate lines;

c) depositing a semiconductor layer over the insulating film;

d) forming a channel protective layer over the semiconductor layer;

e) forming a positive resist layer over the channel protective layer;

f) exposing the positive resist layer to light that has been incident thereon through the backside of the base sub-

strate and then developing the positive resist layer exposed, thereby defining a first resist mask over the gate lines so that the first resist mask is aligned with the gate lines;

g) removing parts of the channel protective layer, which are not covered with the first resist mask, thereby patterning and self-aligning the channel protective layer with the gate lines;

h) depositing a contact layer over the patterned channel protective layer and the semiconductor layer;

i) depositing a conductive film over the contact layer; and

j) patterning the conductive film using a second resist mask, thereby forming not only a data line and a pixel electrode, which both cross a first one of the gate lines, but also a conductive member, which extends from the pixel electrode parallel to the data line and crosses a second one of the gate lines that is adjacent to the first gate line, and then patterning the contact layer, the patterned channel protective layer and the semiconductor layer, thereby defining semiconductor regions for thin-film transistors below the data line and the conductive member so that the upper surface of the semiconductor regions are covered with the patterned channel protective layer.

40. The method of claim 39, wherein the step j) com-

prises:

defining a resist pattern, which includes: relatively thick portions that will define the data line and the conductive member; and a relatively thin portion that will define a region between the data line and the conductive member, as the second resist mask;

etching away parts of the conductive film, the contact layer, the patterned channel protective layer and the semiconductor layer that are not covered with the resist pattern;

removing the relatively thin portion from the resist pattern; and

etching away another part of the conductive film and contact layer, which has been covered with the relatively thin portion of the resist pattern, thereby forming the data line and the conductive member that are separated from each other.

41. The method of claim 39 or 40, wherein before the contact layer is deposited in the step h), the semiconductor layer is patterned and self-aligned with the gate lines by exposing the semiconductor layer to light that has been incident thereon through the backside of the base substrate.

42. The method of claim 40, wherein when the part of the conductive film and contact layer, which has been covered with the relatively thin portion of the resist pattern, is etched

away after the relatively thin portion of the resist pattern has been removed, an exposed part of the semiconductor layer is etched away to leave the semiconductor regions for the thin-film transistors under the patterned channel protective layer.

43. A method of making an active matrix substrate, comprising the steps of:

a) depositing a semiconductor film over a base substrate;

b) depositing a first conductive film over the semiconductor film;

c) patterning the first conductive and semiconductor films, thereby forming a plurality of data lines, a plurality of pixel electrodes and a plurality of conductive members so that parts of the semiconductor film, located between each said data line and associated ones of the conductive members, are not removed but left, wherein each said conductive member extends from associated one of the pixel electrodes along associated one of the data lines;

d) depositing an insulating film over the base substrate;

e) depositing a second conductive film over the insulating film; and

f) patterning the second conductive film, thereby forming

a plurality of gate lines, which cross the data lines, the pixel electrodes and the conductive members, and etching away the parts of the semiconductor film located between each said data line and the associated conductive members entirely except some of the parts of the semiconductor film that are located under the gate lines.

44. The method of claim 43, wherein the step c) comprises:

defining a resist mask, which includes: relatively thick portions that will define the data lines, the pixel electrodes and the conductive members; and relatively thin portions, each of which will define a region between associated one of the data lines and associated ones of the conductive members;

etching away parts of the first conductive and semiconductor films that are not covered with the resist mask;

removing the relatively thin portions from the resist mask; and

etching away other parts of the first conductive film, which have been covered with the relatively thin portions of the resist mask.

45. A method of making an active matrix substrate, comprising the steps of:

a) forming a gate electrode on a base substrate;

b) forming a gate insulating film that covers the gate electrode;

c) depositing a semiconductor layer over the gate insulating film;

d) forming a positive resist layer over the semiconductor layer;

e) exposing the positive resist layer to light that has been incident thereon through the backside of the base substrate and then developing the positive resist layer exposed, thereby defining a first resist mask over the gate electrode so that the first resist mask is aligned with the gate electrode;

f) removing parts of the semiconductor layer, which are not covered with the first resist mask, thereby patterning and self-aligning the semiconductor layer with the gate electrode so that the patterned semiconductor layer includes a semiconductor region for a thin-film transistor;

g) removing the first resist mask;

h) depositing a conductive film over the patterned semiconductor layer; and

i) patterning the conductive film using a second resist mask, thereby forming source and drain electrodes, which both cross the gate electrode, and then further patterning the patterned semiconductor layer, thereby defining the semiconductor region for the thin-film transistor below the source

and drain electrodes.

46. The method of claim 45, wherein the step i) comprises:

defining a resist pattern, which includes: relatively thick portions that will define the source and drain electrodes; and a relatively thin portion that will define a region between the source and drain electrodes, as the second resist mask;

etching away parts of the conductive film and the patterned semiconductor layer that are not covered with the resist pattern;

removing the relatively thin portion from the resist pattern; and

etching away another part of the conductive film, which has been covered with the relatively thin portion of the resist pattern, thereby forming the source and drain electrodes.

47. The method of claim 45 or 46, wherein the source electrode is a part of a data line that extends linearly and crosses the gate electrode, while the drain electrode extends from a pixel electrode parallel to the data line.

48. A method of making an active matrix substrate, comprising the steps of:

a) forming a gate electrode on a base substrate;

b) forming a gate insulating film that covers the gate electrode;

c) depositing a semiconductor layer over the gate insulating film;

d) forming a channel protective layer over the semiconductor layer;

e) forming a first positive resist layer over the channel protective layer;

f) exposing the first positive resist layer to light that has been incident thereon through the backside of the base substrate and then developing the first positive resist layer exposed, thereby defining a first resist mask over the gate electrode so that the first resist mask is aligned with the gate electrode;

g) removing parts of the channel protective layer, which are not covered with the first resist mask, thereby patterning and self-aligning the channel protective layer with the gate electrode;

h) depositing a contact layer over the patterned channel protective layer and the semiconductor layer;

i) defining a second resist mask over the gate electrode;

j) removing parts of the contact and semiconductor layers, which are not covered with the second resist mask,

thereby patterning and self-aligning the contact layer, the patterned channel protective layer and the semiconductor layer, including a portion to be a semiconductor region for a thin-film transistor, with the gate electrode;

k) removing the second resist mask;

l) depositing a conductive film over the patterned contact layer; and

m) patterning the conductive film using a third resist mask, thereby forming source and drain electrodes, which both cross the gate electrode, and further patterning the patterned contact, channel protective and semiconductor layers, thereby defining the semiconductor region for the thin-film transistor below the source and drain electrodes so that the upper surface of the semiconductor region is partially covered with the patterned channel protective layer.

49. The method of claim 48, wherein the step m) comprises:

defining a resist pattern, which includes: relatively thick portions that will define the source and drain electrodes; and a relatively thin portion that will define a region between the source and drain electrodes, as the third resist mask;

etching away parts of the conductive film and the patterned contact and semiconductor layers that are not covered

with the resist pattern;

removing the relatively thin portion from the resist pattern; and

etching away another part of the conductive film and contact layer, which has been covered with the relatively thin portion of the resist pattern, thereby forming the source and drain electrodes that are separated from each other.

50. The method of claim 48 or 49, wherein the channel protective layer is patterned to have a width narrower than that of the semiconductor region.

51. A method of making an active matrix substrate, comprising the steps of:

a) forming a gate electrode on a base substrate;

b) forming a gate insulating film that covers the gate electrode;

c) depositing a semiconductor layer over the gate insulating film;

d) forming a channel protective layer over the semiconductor layer;

e) forming a positive resist layer over the channel protective layer;

f) exposing the positive resist layer to light that has been incident thereon through the backside of the base sub-

strate and then developing the positive resist layer exposed, thereby defining a first resist mask over the gate electrode so that the first resist mask is aligned with the gate electrode;

g) removing parts of the channel protective layer, which are not covered with the first resist mask, thereby patterning and self-aligning the channel protective layer with the gate electrode;

h) depositing a contact layer over the patterned channel protective layer and the semiconductor layer;

i) depositing a conductive film over the contact layer; and

j) patterning the conductive film using a second resist mask, thereby forming source and drain electrodes, which both cross the gate electrode, and further patterning the contact, channel protective and semiconductor layers, thereby defining a semiconductor region for a thin-film transistor below the source and drain electrodes so that the upper surface of the semiconductor region is partially covered with the patterned channel protective layer.

52. The method of claim 51, wherein the step j) comprises:

defining a resist pattern, which includes: relatively thick portions that will define the source and drain elec-

trodes; and a relatively thin portion that will define a region between the source and drain electrodes, as the second resist mask;

etching away parts of the conductive film and the contact and semiconductor layers that are not covered with the resist pattern;

removing the relatively thin portion from the resist pattern; and

etching away another part of the conductive film and contact layer, which has been covered with the relatively thin portion of the resist pattern, thereby forming the source and drain electrodes that are separated from each other.

53. The method of claim 51 or 52, wherein before the contact layer is deposited in the step h), the semiconductor layer is patterned and self-aligned with the gate electrode by exposing the semiconductor layer to light that has been incident thereon through the backside of the base substrate.

54. The method of claim 52, wherein when the part of the conductive film and contact layer, which has been covered with the relatively thin portion of the resist pattern, is etched away after the relatively thin portion of the resist pattern has been removed, an exposed part of the semiconductor layer is etched away to leave the semiconductor region for the thin-

film transistor under the channel protective layer.

55. A thin-film transistor comprising:

a substrate;

a gate electrode formed on the substrate;

a gate insulating film formed over the gate electrode;

a semiconductor layer formed over the gate electrode with the gate insulating film interposed therebetween;

a source electrode crossing the semiconductor layer; and

a drain electrode crossing the semiconductor layer,

wherein side faces of the semiconductor layer, which are parallel to a direction in which the source and drain electrodes extend, are aligned with outer side faces of the source and drain electrodes.

56. The transistor of claim 55, wherein the other side faces of the semiconductor layer, which are parallel to a direction in which the gate electrode extends, are aligned with side faces of the gate electrode.

57. The transistor of claim 55 or 56, wherein a contact layer exists between the source electrode and the semiconductor layer and between the drain electrode and the semiconductor layer.

58. A thin-film transistor comprising:

a substrate;

a gate electrode formed on the substrate;

a gate insulating film formed over the gate electrode;

a semiconductor layer formed over the gate electrode with the gate insulating film interposed therebetween;

a channel protective layer formed on the semiconductor layer;

a source electrode crossing the channel protective layer; and

a drain electrode crossing the channel protective layer,

wherein side faces of the channel protective layer, which are parallel to a direction in which the source and drain electrodes extend, are aligned with outer side faces of the source and drain electrodes.

59. The transistor of claim 58, wherein the other side faces of the channel protective layer, which are parallel to a direction in which the gate electrode extends, are spaced apart from each other by a distance smaller than the line width of the gate electrode.

60. The transistor of claim 58 or 59, wherein side faces of the semiconductor layer, which are parallel to the direction in which the gate electrode extends, are aligned with

the side faces of the gate electrode.

61. The transistor of claim 60, wherein the other side faces of the semiconductor layer, which are parallel to the direction in which the source and drain electrodes extend, are aligned with the outer side faces of the source and drain electrodes.

62. The transistor of claim 58, wherein a contact layer exists between the source electrode and the semiconductor layer and between the drain electrode and the semiconductor layer.